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TBM Test Setup

1. Introduction

The test setup for the Token Bit Manager ASIC (TBM) consists of the following items:

- Cascade/Alessi 6171 semi-automatic 8 “ chuck probe station
- EED ASIC Test System
- TBM Interface Board
- TBM Buffer Board
- TBM Adapter Board
- TBM Probe Card

The last four items in the above list are custom designs specific for the TBM chip. The TBM Adapter Board with a wire-bonded chip attached to it is designed to replace the TBM Probe Card to simplify software development.

2. Functional Block-Diagram

A simplified block-diagram of the setup is shown in the Figure 1.

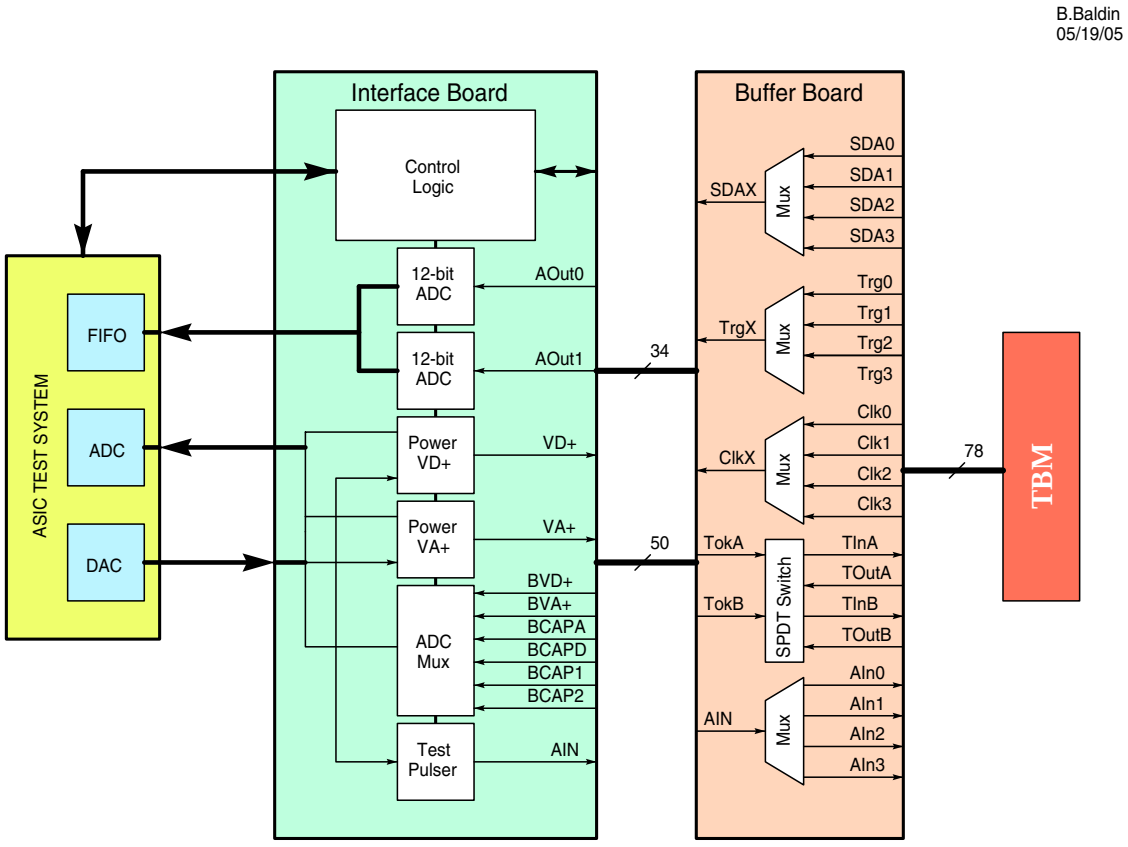

Figure 1 A Block-Diagram of the TBM Test Setup

The Interface Board is located next to the ASIC Test System box and has short cable connections to it. The Buffer Board is placed on the top of the TBM Probe Card and is connected by two flat cables (6 ft., 34 and 50 wires) to the Interface Board. The TBM Probe Card is mounted in the probe station. During software development the TBM Adapter Board replaces the probe card to eliminate the need to use a probe station.

The Interface Board includes two 12-bit high speed ADCs connected to two TBM analog outputs. Each ADC output is independently sampled into the ASIC Test System FIFO memory. Four 8-bit wide memories are used for this purpose. ADC information is stored in the FIFOs only during time intervals between trigger and Token In or between Token Out of the TBM and Token In. The Control Logic generates trigger and Token In signals at arbitrary selected clock cycles (0..255). The number of ADC samples stored in the memory is determined by a delay between selected start signal (trigger or Token Out) and Token In signal. There is no provision to prevent memory overflow or reading empty memory, therefore, it is recommended that full and empty flags are tested by software before and after reading out information from the FIFOs. It is also possible to measure a shape of the TBM output signal by using uniformly shifted ADC clock. The step of the shift is approximately 2 nS, which allows for a coarse signal transition time measurement.

The Interface Board has two programmable power supplies with shutdown (0..4.5V, 300 mA) to provide independent 2.5V power outputs for the TBM's digital and analog portions. The power supplies are controlled by the ASIC Test System DACs (DAC0 and DAC1). Each power supply has a current measurement output, which is read out by ADC1 and ADC2 respectively. Outputs of the voltage regulators and bypass cap pads are connected to the analog multiplexer and are read out by the ADC0. Six voltages are measured directly on the chip: VD+, VA+, ACap, DCap, CapA and CapB.

The Test Pulser generates a square pulse of variable amplitude controlled by DAC2. The output of the Test Pulser is multiplexed to four TBM analog inputs AIn0..AIn3. This feature allows linearity measurements of the individual TBM inputs.

Two TBM token outputs can be simultaneously switched to the token inputs for internal loop test. The token outputs are always latched by the Control Logic. If there is no token output within certain amount of time after the trigger, an error bit will be set in the status register.

TBM's ROC control signal outputs (SDA0..SDA3, TRG0..TRG3, CLK0..CLK3) are multiplexed into three Control Logic inputs. The presence of the signal transitions is latched in a separate bit of the status register. The register must be cleared after switching the multiplexer to the desired channel.

The Control Logic generates necessary timing and control signals at the fixed clock frequency of 40 MHz. Serial command interface uses three 8-bit registers to form a command (see Token Bit Manager 04 Chip Documentation). The returned data is stored in internal FIFO memory and can be read out in a byte format via ASIC Test System inputs DCI8..DCI15. An 8-bit status register as well as other internal registers are read out using DCI0..DCI7 inputs. An internal timing sequencer generates trigger signal based on the value of a three-bit register. Each trigger signal can be followed by a token with adjustable delay as described above to simulate the ROC chain. As in the previous project

for PSI46 testing, DCO0..DCO7 lines are used as an 8-bit input data bus and pulsed lines 0..15 are used as address lines and to trigger specific functions (e.g. generate serial interface command).

3. Reference

E.Bartz, “Token Bit Manager 04 Chip Documentation”, version 0.9.5.1 - http://www.physics.rutgers.edu/~bartz/cms/tbm2/0.25u/TBM_Documentation_0.9.pdf